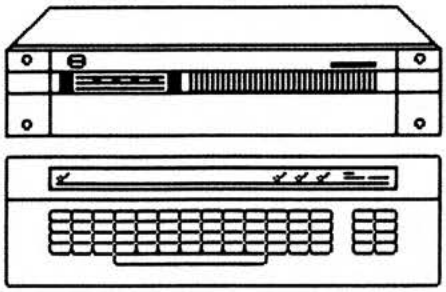
NABU



Technical Manual

MJP

HARDWARE INFORMATION

General Description

The Home Cable Computer (HCC) processor board is a general purpose single board computer. Based on a Z80A microprocessor it has 64K of on board dynamic RAM. The HCC is designed to operate in a home setting, using the standard color or monochrome television set as a display and sound output device.

The processor board is approximately 9.626" by 12". It provides interfaces to the Home Cable Computer Adapter (HCCA), the four option card slots, and the detachable keyboard.

The processor board is mounted just above, and parallel to, the bottom of the HCC basic package. A steel bulkhead plate is mounted across the back edge of the board in the vertical plane. This bulkhead has all external interface connectors mounted on it, providing for RF shielding and strain relief. When the processor board is installed in the HCC basic package, the bulkhead is screwed to the inside back surface with the connectors protruding through rectangular slots in the rear of the package. Thus, the bulkhead is electrically part of the steel package and effectively eliminates RF radiation to the outside.

Clocks

The processor board is designed to operate in a television environment requiring specific clock frequencies. The processor board has a 10.738635 megahertz $\pm$ 50 ppm fundamental frequency, parallel-mode crystal. This is directly connected to the video processor. The video processor divides the clock frequency by three resulting in a 3.579545 (referred to hereafter as 3.58) megahertz basic clock rate. This 3.58 megahertz clock is used to drive the Z80A microprocessor.

Z80A Microprocessor

The processor board contains a Z80A microprocessor. In addition to application software, it controlls the overall HCC system and has inherent dynamic RAM refresh capability.

ROM

A 4K byte ROM (Read Only Memory) contains the bootstrap software. Upon reset, this software performs a minimal self test on the processor board and initializes the system. It also contains software which can communicate with the HCCA or a floppy disk to allow for bootstrapping.

The ROM may be selected or deselected under software control. When selected, any memory read request to addresses 0000 - 0FFF hex will be directed to the ROM; write requests to these addresses will go to RAM.

RAM

The processor board contains 64K bytes of RAM (Random Access Memory), available to the CPU. The memory consists of eight 64K x 1 dynamic RAM chips, refreshed automatically by the Z80A.

Address Decoder

This logic provides all memory mapping and I/O address decoding.

Video Processor

The HCC processor board uses the TMS9918A video display processor chip. This processor generates NTSC compatible color video signal.

The video processor is connected to the Z80A data bus and resides in I/O space. The video processor controls its own 16K x 8 dynamic RAM refresh memory which is not connected to the Z80A data bus. The Z80A issues commands to the video processor to control it and can read or write the refresh RAM through the video processor.

The output of the video processor is connected to the RF modulator for display on the television set. This output is also available on another connector as NTSC compatible video signal, which can drive a video monitor.

For more details, refer to the TMS9918A Video Processor Data Manual.

Audio Processor

The HCC processor board contains an AY-3-8910 programmable sound generator chip. This chip produces three channels of sound used in applications such as sound effects, music synthesis, alarms, and FSK modems.

The sound generator is programmed by the Z80A to produce the desired audio waveforms. For more detail, see the AY-3-8910/8912 Programmable Sound Generator Data Manual.

In order to use the speaker of the television set, the output of the sound generator is connected to the RF modulator. In addition, the audio output is available on a connector for transmission to an external amplifier.

The AY-3-8910 contains two 8-bit bi-directional parallel ports. One is used to output the interrupt masks; the other, to read the status flags.

RF Modulator

The RF modulator combines the NTSC compatible video signal from the video processor with the sound generator output. The resulting signal can be received on channel 3 or 4 of a standard home television set. The selection of channel 3 or 4 is made by an internal switch mounted on the processor board.

The RF output impedance is 75 ohms. For connection to 300 ohm television antenna input terminals, an external impedance matching balum must be used.

RF Switch

Since the HCC is usually functioning in a CATV environment, provisions must be made to accommodate a cable converter signal as well as the RF output from the HCC.

To accomplish this, the HCC processor board has an external RF input connector. Either the external signal or the processor signal may be selected by a video switch and transmitted to the RF output connector. This output is connected to the antenna input of the TV set. The computer can switch between the two RF sources under program control. If the HCC power is off, the external input is selected automatically.

Note: The RF switch cannot carry a raw CATV signal due to bandwidth limitations; the switch is designed to carry channel 3 or 4 only.

Keyboard Interface

This interface supplies unregulated +10 volt DC power to the detachable keyboard and receives serial data from the keyboard. The keyboard contains a single chip microprocessor which performs keyboard encoding and games control. The keyboard output is received by the HCC 8251 programmable communications interface. The data rate is 6992 baud using EIA RS422 transmission over twisted pair cable with overall shield.

Printer Interface

The printer interface is capable of driving a subset of the standard Centronics parallel printer.

The printer is accessed through a parallel port with 8 data lines. It is connected to the HCC via a 15 pin, female, D-type connector.

HCCA Interface

The HCCA interface consists of a full duplex, 111 kilobit per second serial interface using EIA RS422 transmission. The processor can send commands to the HCCA, requesting data or programs from the device connected.

Option Card Interface

This interface provides bi-directional data, address and control signals to up to four option cards, which can be installed in the basic HCC package. Each card is assigned 16 consecutive I/O addresses as follows:

a) slot 0 - addresses C0 to CF
b) slot 1 - addresses D0 to DF
c) slot 2 - addresses E0 to EF
d) slot 3 - addresses F0 to FF

The buffered signal bus is brought to four sets of pins at the front edge of the processor board. Each option card is connected to one set of pins by a flexible cable with an inline female connector.

Interrupt Logic

The processor board permits eight levels of maskable, vectored-priority interrupts. The interrupts are vectored using Z80 mode 2. Each interrupt level is masked by a bit in the sound processor port A. They are listed in order of decreasing priority as follows:

0) HCCA Receive
1) HCCA Send
2) Detachable Keyboard
3) Video Frame Sync
4) Option Card 0
5) Option Card 1
6) Option Card 2
7) Option Card 3

Reset Switch

A momentary contact pushbutton switch is mounted on the front of the chassis to provide for a system reset.

Control Register

A register is provided to permit software control of the following devices:

a) 3 LED's mounted on the front panel
b) ROM enable
c) RF switch
d) Printer data strobe

Status Byte

A status byte can be read by the Z80 via the sound processor port B. The status flags are listed in PROGRAMMING INFORMATION, Sound Generator.

PROGRAMMING INFORMATION

Device Addresses

DEVICE	ADDRESS
Control Register	00H (write only)
Sound Generator	
I/O Port A	40H (write data)
-interrupt enable	41H (latch address)
I/O Port B	40H (read data)
-status	
HCCA	80H (read/write)
Keyboard	90H (data)
	91H (status)
VDP	A0H (data transfer)
	A1H (latch address)
Printer I/O Port	B0H (write only)

Control Register

D7 - N.C.	
D6 - N.C.	
D5 - Yellow LED	-(Pause)
D4 - Red LED	-(Alert)
D3 - Green LED	-(Check)
D2 - Data Strobe	-strobes data to the printer register
D1 - Video Switch	-chooses the signal for transmission to the TV screen
D0 - ROM Select	-selects 4K ROM

Printer I/O Port

(MSB)							(LSB)	
D7	D6	D5	D4	D3	D2	D1	D0	-B0H (write data only)

Sound Generator See AY-3-8910/8912 data manual.

In addition to sound generation, I/O ports A and B are used to provide the following functions:

Interrupt Enable (Output) -Port A (write only)

D7 - HCCA Receive
D6 - HCCA Send
D5 - Keyboard
D4 - Video Frame Sync
D3 - Option Card 0 (J9)
D2 - Option Card 1 (J10)
D1 - Option Card 2 (J11)
D0 - Option Card 3 (J12)

Status Byte (Input) -Port B (read only)

D7 - N.C.
D6 - Overrun Error (HCCA UART)
D5 - Framing Error (HCCA UART)
D4 - Printer Busy
D3 - A2 Priority
D2 - A1 Priority
D1 - A0 Priority
D0 - Interrupt Request

Note: If 'Interrupt Request' (D0) is true, A2 - A0 contains the number of the highest interrupt request (0 is the highest priority).

Keyboard See 8251A data manual.

90H (Data)
91H (Status)

HCCA See TR1863 data manual.

80H (Read Data)
80H (Write Data)

VDP See TMS9918A data manual.

A0H (Data Transfer)
A1H (Latch Address)

INTERFACES

Non-interchangeable connectors have been used whenever damage could result from incorrect connections.

Printer Interface

A fifteen pin female D-type connector is used.

Pin	Signal	Direction	Description
1	STROBE	Out	Strobe pulse to output data. Pulse width must be > 0.5 uS at receiving end.
2	DATA 1	Out	Data Bit 1 (LSB)
3	DATA 2	Out	Data Bit 2
4	DATA 3	Out	Data Bit 3
5	DATA 4	Out	Data Bit 4
6	DATA 5	Out	Data Bit 5
7	DATA 6	Out	Data Bit 6
8	DATA 7	Out	Data Bit 7
9	DATA 8	Out	Data Bit 8
11	BUSY	In	Indicates the printer cannot receive data as follows: 1) During data loading 2) During print operation 3) In OFF-LINE state 4) During printer error state
15	0V	-	Logic ground.

Phono Type Connectors

RCA Female Phono connectors are used for the following interfaces:

a) Video out
b) Audio out

HCCA

A 5-pin DIN connector is used as follows:

Pin	Description
5	Transmit +
3	Transmit -
1	Receive +
4	Receive -

Keyboard

A 6-pin DIN connector is used as follows:

Pin	Description	
1	unused	(Shield = GND)
2	+9 volts return	
3	+9 volts	
4	TX+	
5	TX-	
6	unused	

LED

An 8-pin in-line header is used to interconnect the LED/Reset Switch PCB with the HCC processor board as follows:

Pin	Description
1	Power On (green)
2	Pause (yellow)
3	Alert (red)
4	Check (green)
5	Reset Switch
6	Logic Ground

Option Card

Four 30-pin in-line headers are used to provide signal interconnections to the option cards as follows:

Pin	Signal	Direction	Description
16	D0	In/Out	Data Bit 0 (LSB)
17	D1	In/Out	Data Bit 1
18	D2	In/Out	Data Bit 2
19	D3	In/Out	Data Bit 3
20	D4	In/Out	Data Bit 4
21	D5	In/Out	Data Bit 5
22	D6	In/Out	Data Bit 6
23	D7	In/Out	Data Bit 7
05	CS*	Out	Option card select. One per slot where * is the slot number.
06	A0	Out	Address Bit 0
07	A1	Out	Address Bit 1
08	A2	Out	Address Bit 2
09	A3	Out	Address Bit 3
11	WR	Out	Write
12	RD	Out	Read
13	IORQ	Out	I/O Request
01	INT*	In	Interrupt request from option card in slot *.
02	INTAK	Out	Interrupt acknowledge
14	WAIT*	In	Wait request from option card in slot *. Note: WAIT 0 - WAIT 3 are open collector input.
15	RESET	Out	System reset
04	AUDIO*	In	Audio signal from option card in slot *. Note: AUDIO 0 - AUDIO 3 must be AC coupled and not exceed 5Vpp.
03	3.58Mhz	Out	System clock
10	1.79Mhz	Out	
24	+5V	Out	
25	+5V	Out	
29	+12V	Out	
30	-12V	Out	
26	GND		
27	GND		
28	GND		

POWER SUPPLY

Unit	AC/DC Multiple Output Switching Power Supply
Model	AC8152 (ASTEC) or MRM146U (TDK)
AC Input Voltage	95 - 135 VAC
AC Input Frequency	57 to 63 Hz
AC Input Current	Less than 1.0A
AC Inrush Current	30A maximum half cycle peak current at 115 VAC.
DC Output Power	40 Watts

DC Output Voltage

Pin	Signal	InternalConnectors (J7,J8,J9)
4	+05.0V	+5% Tol. for 0.45 to 2.5A
2	+12.0V	+5% Tol. for 0.30 to 2.0A
1	-12.0V	for 0.00 to 0.1A
3	Com	

AC Ripple

Output #1	(+5V)	50 mVp-p
Output #2	(+12V)	150 mVp-p
Output #3	(-12V)	150 mVp-p

Individual Maximum Output Current

Output #1	(+5V)	5.0A
Output #2	(+12V)	2.5A
Output #3	(-12V)	0.5A

Overvoltage Protection	5.8V min. to 6.8V max. (+5V only)
Overcurrent Protection	All outputs short circuit protected

Environmental Characteristics

Operating temperature	10 C to 35 C
Storage Temperature	-20 C to 70 C
Relative Humidity	10% to 90% (non-condensing)

KEYBOARD INFORMATION

General Description

The HCC keyboard is a peripheral device connected to the HCC by a 4 wire shielded cable. The cable provides power to the keyboard and transmits the serial output signal to the HCC. The keyboard assembly is housed in a two piece plastic housing containing 1 logic board.

Microprocessor

MC6801 -2048 bytes ROM/128 bytes RAM
-29 parallel I/O & 2 control lines
-3 function 16-bit programmable timer
-full duplex serial communications interface
-3 fundamental operating modes (uses mode 1)
-internal clock generator
-enhanced 8-bit MC6800 MPU

Filter

The joysticks are remote from the keyboard enclosure by approximately 1.5 meters of cable. A filter must be added to protect the MPU from static discharge and also to prevent RF radiation from emitting from the joystick cables.

Software Interface

The internal operating software in the HCC reads a byte-wide read-only data register to obtain data from the keyboard passed on the serial link. This implies all data/commands from the keyboard are sent as 8-bit bytes.

Hardware Interface

Output from the remote keyboard will be via a two wire differential signal method similar to that described in EIA RS-422. Cable type will be a two pair 22 AWG overall shielded jacketed cable with a maximum length of 20 feet. The 6-pin DIN connector also supplies power to the keyboard from the HCC (+9 volts unregulated @200 mA).

Pin	Function	
1	unused	(Shield = GND)
2	+9 volts return	
3	+9 volts	
4	TX +	
5	TX -	
6	unused	

Game Controller Interface

Game control connectors are 9-pin sub-miniature "D" type right angle mounted plug (male pin) connectors.

Pin	Function
1	Up Contact
2	Down Contact
3	Left Contact
4	Right Contact
5	Unused
6	Fire Control Contact
7	Unused
8	GND
9	Unused

Keyboard/HCC Communication Protocol

All information is transmitted as 8-bit bytes. The Keyboard Encoding Chart shows the encoding of data transmitted from the keyboard. Note that special function keys are always encoded with their high bit set. The keyboard only transmits information when a data value changes. Also, in the case of the key switches and game controller digital contacts, the keyboard only transmits debounced data. That is to say, the keyboard indication of an event guarantees that the event did indeed occur.

Game Controller Command Byte Format

The following illustrates the HCC/KBD protocol. Game controller information is transmitted by proceeding the actual data with a command byte which indicates which device the data come from. Currently defined device command bytes are:

80H JS1 - following byte is digital data from game controller port 1
81H JS2 - following byte is digital data from game controller port 2

Digital Contact (Joystick) Byte Format

Digital contact information (one 8-bit byte) is transmitted immediately after the relevant device command byte. All digital contacts on a game controller are transmitted if the state of a single contact changes. It is assumed that the digital contacts are all zero when not being used. Whenever a contact is made the corresponding bit in the data byte is set to one. As shown in the Keyboard Encoding Chart, column "A0-B0" are saved for digital contact (joystick) 'JS' device data. In byte format shown below, bits 5-7 are fixed values (header). If fire button (F) is

clear "Ax" is transmitted. If fire button (F) is set "Bx" is transmitted. Where "x" is the digital contact position.

Digital Contact (Joystick) Data Byte Format

D7	1	Fixed Header
D6	0	Fixed Header
D5	1	Fixed Header
D4	F	Fire Button
D3	U	Up Contact
D2	R	Right Contact
D1	D	Down Contact
D0	L	Left Contact

Keyboard Encoding

The keyboard encoding is shown in the Keyboard Encoding Chart. The keyboard is scanned using the "third key lock-out algorithm", which provides automatic repeat at an exponentially increasing rate on the keys held down, up to a maximum of two keys. Keys: ESC, SHIFT, CTRL, CAPS, and all SPECIAL FUNCTION KEYS are non repeatable. There is no audio feedback in the keyboard unit. If an error condition is detected by the MPU it sends the appropriate error indication to the HCC (see Keyboard Error Message Encoding). Keyboard data is transmitted in a one 8-bit byte format without a preceding command byte.

Control Keys

The following control keys are handled by the keyboard and are defined as follows. These keys have no effect on the keyboard function keys.

SHIFT - when held down causes alphabetic keys to generate capital letters, and other keys to generate the character indication on the upper portion of the key top.

CAPS - a locking key that when held down causes the keyboard to generate capital letters only. Keys other than alphabetic characters are not affected.

CTRL - when held down masks bits 6-7 of the encoded value of any standard ASCII key which is struck.

Special Function Keys (Release Coded)

The keyboard also has a set of special function keys. These keys are not affected by the SHIFT, CAPS, or CONTROL keys, and are not auto-repeatable. These keys send codes when they are depressed as well as when they are released.

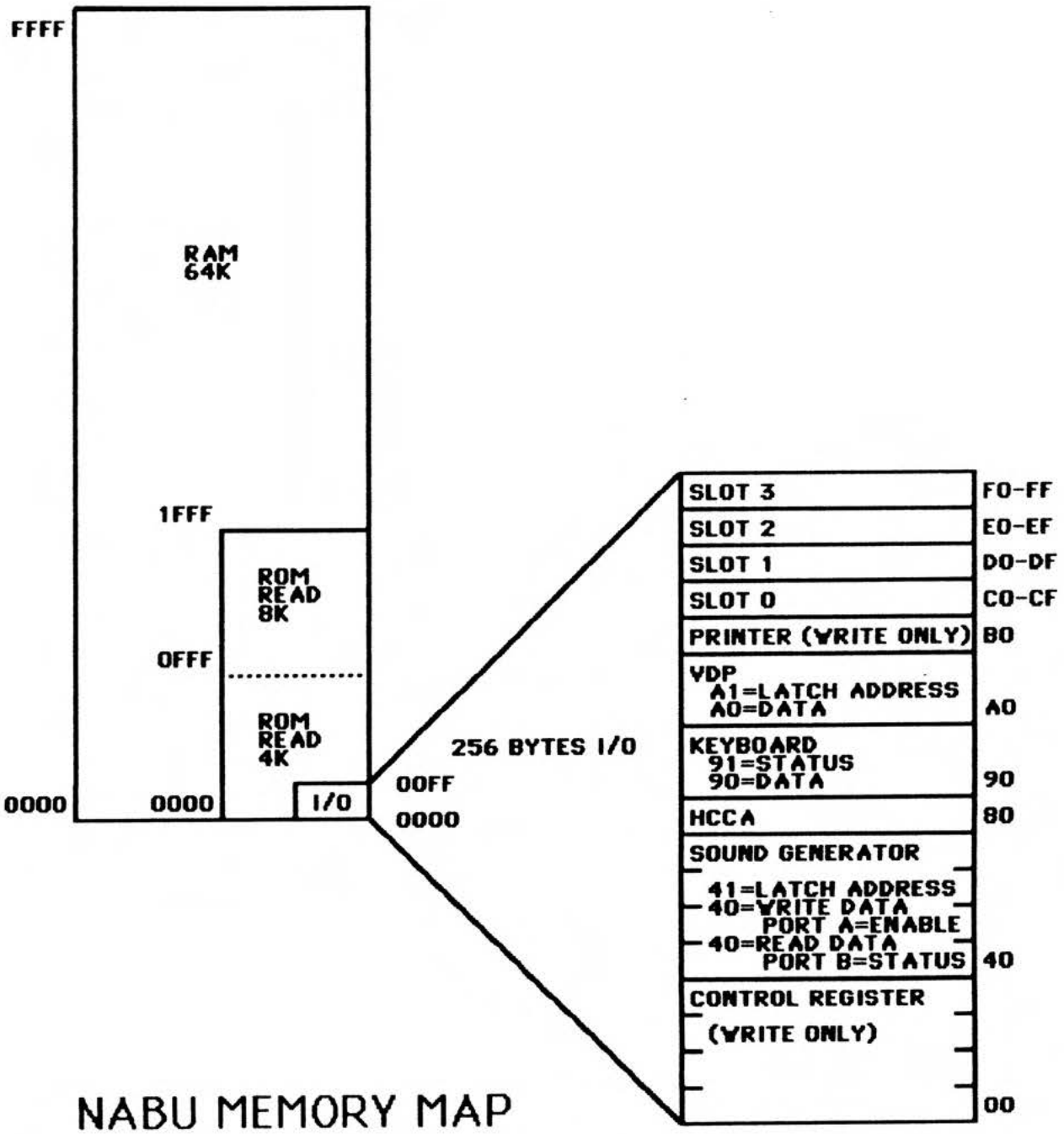
Keyboard Error Message Encoding

As shown in the Keyboard Encoding Chart, addresses 90H - 95H are a set of messages that are sent out the HCC if any prescribed condition exists.

90H	E1	- indicates multiple key depression
91H	E2	- indicates faulty keyboard RAM
92H	E3	- indicates faulty keyboard ROM
93H	E4	- indicates illegal ISR activated
94H	E5	- indicates software "watchdog" - under no-load conditions signal sent out approximately every 3.7 seconds. Signal indicates keyboard functioning correctly.
95H	E6	- indicates power-up/reset when the keyboard is first powered up. However, if for any reason program control is lost, a hardware timer forces a reset which sends "95" again.

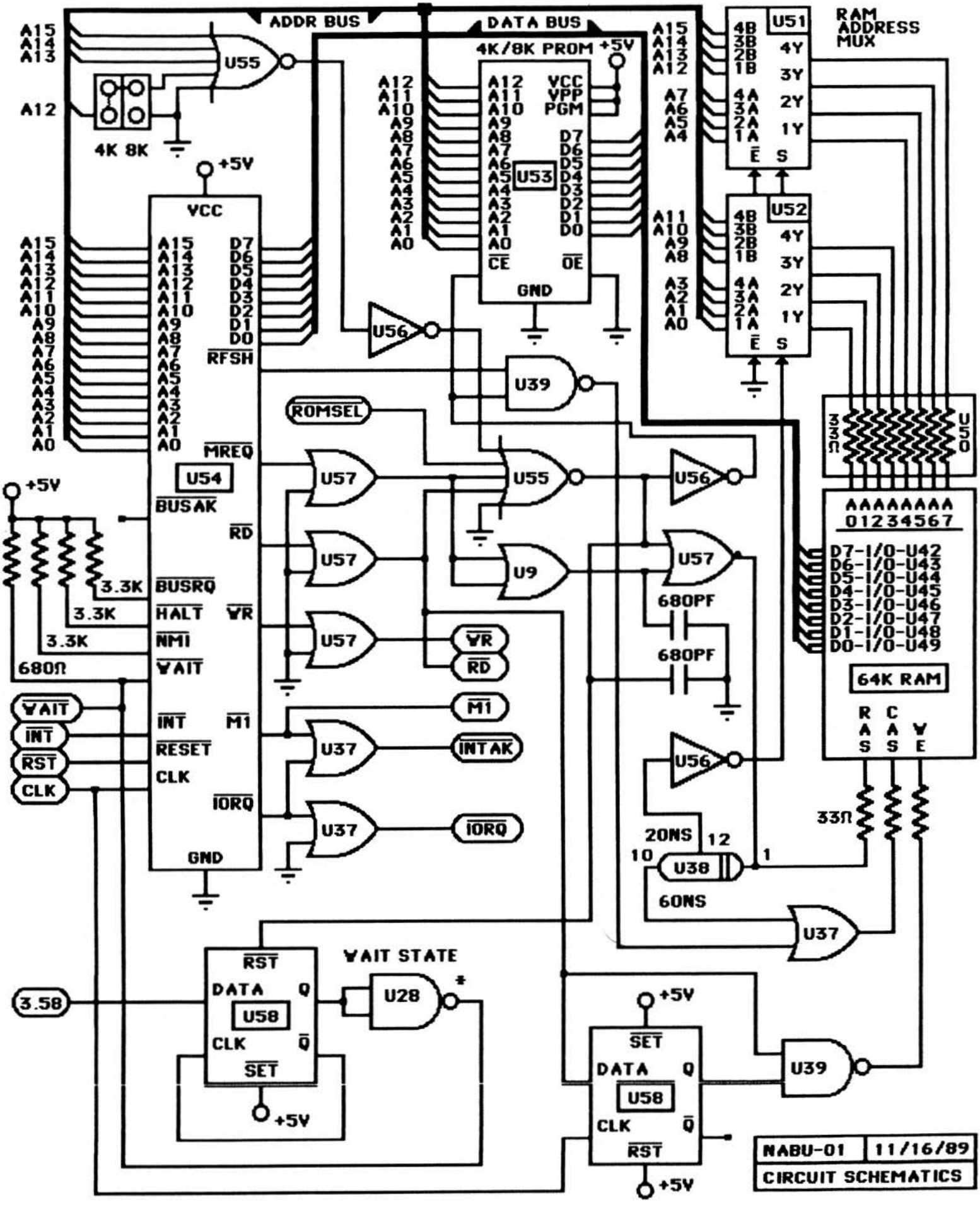
Keyboard Encoding Chart

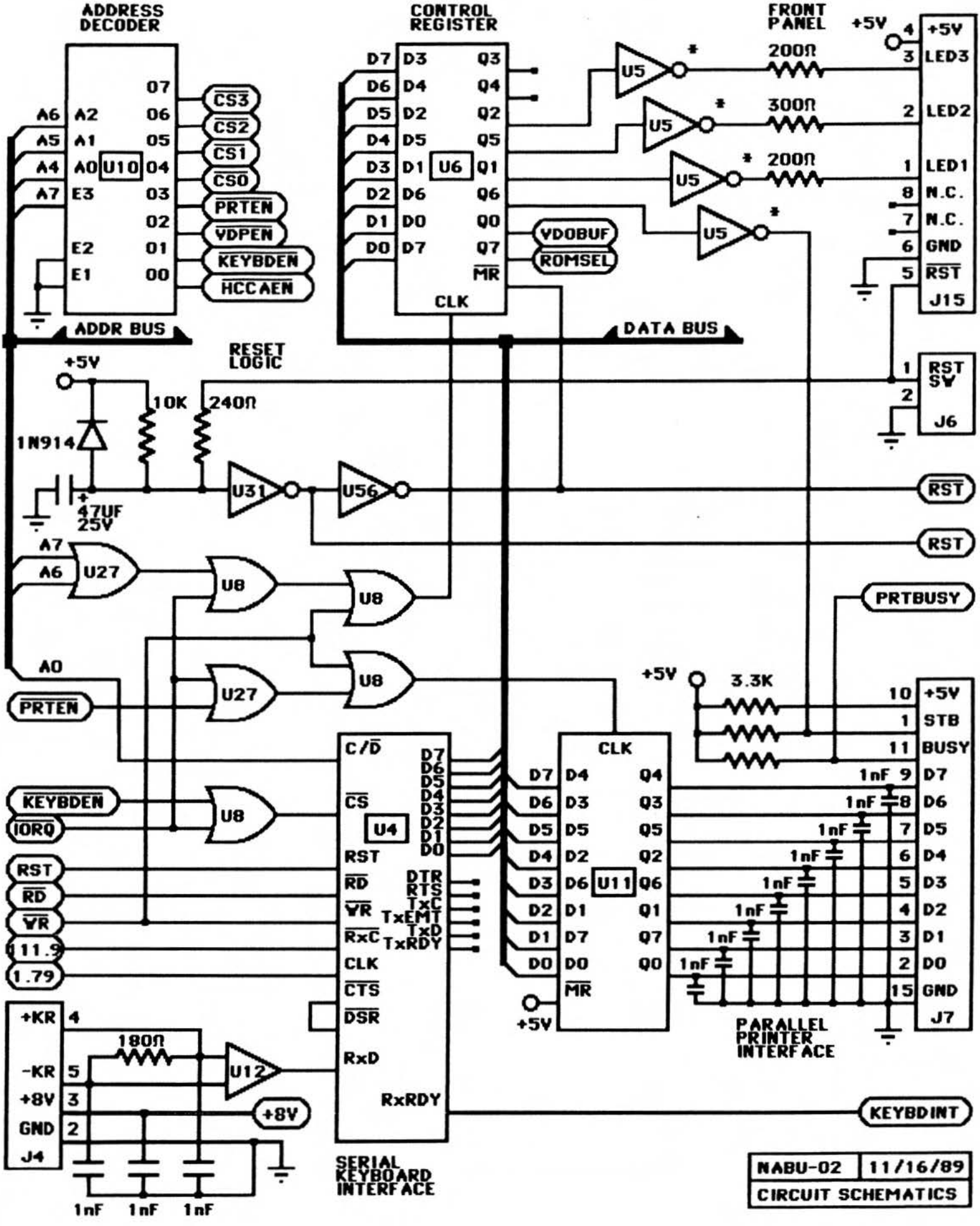
00 ctrl @	20 (SP)	40 @	60 (na)	80 'JS1'	A0 'JS'	C0 (na)	E0 -> (dn)
01 ctrl A	21 !	41 A	61 a	81 'JS2'	A1 'JS'	C1 (na)	E1 <- (dn)
02 ctrl B	22 "	42 B	62 b	82 (na)	A2 'JS'	C2 (na)	E2 I (dn)
03 ctrl C	23 #	43 C	63 c	83 (na)	A3 'JS'	C3 (na)	E3 I (dn)
04 ctrl D	24 $	44 D	64 d	84 (na)	A4 'JS'	C4 (na)	E4 III> (dn)
05 ctrl E	25 %	45 E	65 e	85 (na)	A5 'JS'	C5 (na)	E5 <III (dn)
06 ctrl F	26 &	46 F	66 f	86 (na)	A6 'JS'	C6 (na)	E6 NO (dn)
07 ctrl G	27 '	47 G	67 g	87 (na)	A7 'JS'	C7 (na)	E7 YES (dn)
08 ctrl H	28 (	48 H	68 h	88 (na)	A8 'JS'	C8 (na)	E8 SYM (dn)
09 ctrl I	29)	49 I	69 i	89 (na)	A9 'JS'	C9 (na)	E9 PAUSE (dn)
0A ctrl J	2A *	4A J	6A j	8A (na)	AA 'JS'	CA (na)	EA TV/NABU (dn)
0B ctrl K	2B +	4B K	6B k	8B (na)	AB 'JS'	CB (na)	EB (na)
0C ctrl L	2C ,	4C L	6C l	8C (na)	AC 'JS'	CC (na)	EC (na)
0D ctrl M	2D -	4D M	6D m	8D (na)	AD 'JS'	CD (na)	ED (na)
0E ctrl N	2E .	4E N	6E n	8E (na)	AE 'JS'	CE (na)	EE (na)
0F ctrl O	2F /	4F O	6F o	8F (na)	AF 'JS'	CF (na)	EF (na)
10 ctrl P	30 0	50 P	70 p	90 'E1'	B0 'JS'	D0 (na)	F0 -> (up)
11 ctrl Q	31 1	51 Q	71 q	91 'E2'	B1 'JS'	D1 (na)	F1 <- (up)
12 ctrl R	32 2	52 R	72 r	92 'E3'	B2 'JS'	D2 (na)	F2 I (up)
13 ctrl S	33 3	53 S	73 s	93 'E4'	B3 'JS'	D3 (na)	F3 I (up)
14 ctrl T	34 4	54 T	74 t	94 'E5'	B4 'JS'	D4 (na)	F4 III> (up)
15 ctrl U	35 5	55 U	75 u	95 'E6'	B5 'JS'	D5 (na)	F5 <III (up)
16 ctrl V	36 6	56 V	76 v	96 (na)	B6 'JS'	D6 (na)	F6 NO (up)
17 ctrl W	37 7	57 W	77 w	97 (na)	B7 'JS'	D7 (na)	F7 YES (up)
18 ctrl X	38 8	58 X	78 x	98 (na)	B8 'JS'	D8 (na)	F8 SYM (up)
19 ctrl Y	39 9	59 Y	79 y	99 (na)	B9 'JS'	D9 (na)	F9 PAUSE (up)
1A ctrl Z	3A :	5A Z	7A z	9A (na)	BA 'JS'	DA (na)	FA TV/NABU (up)
1B ctrl [	3B ;	5B [	7B {	9B (na)	BB 'JS'	DB (na)	FB (na)
1C ctrl <	3C <	5C (na)	7C (na)	9C (na)	BC 'JS'	DC (na)	FC (na)
1D ctrl]	3D =	5D]	7D }	9D (na)	BD 'JS'	DD (na)	FD (na)
1E ctrl ^	3E >	5E ^	7E (na)	9E (na)	BE 'JS'	DE (na)	FE (na)
1F ctrl -	3F ?	5F -	7F DEL	9F (na)	BF 'JS'	DF (na)	FF (na)

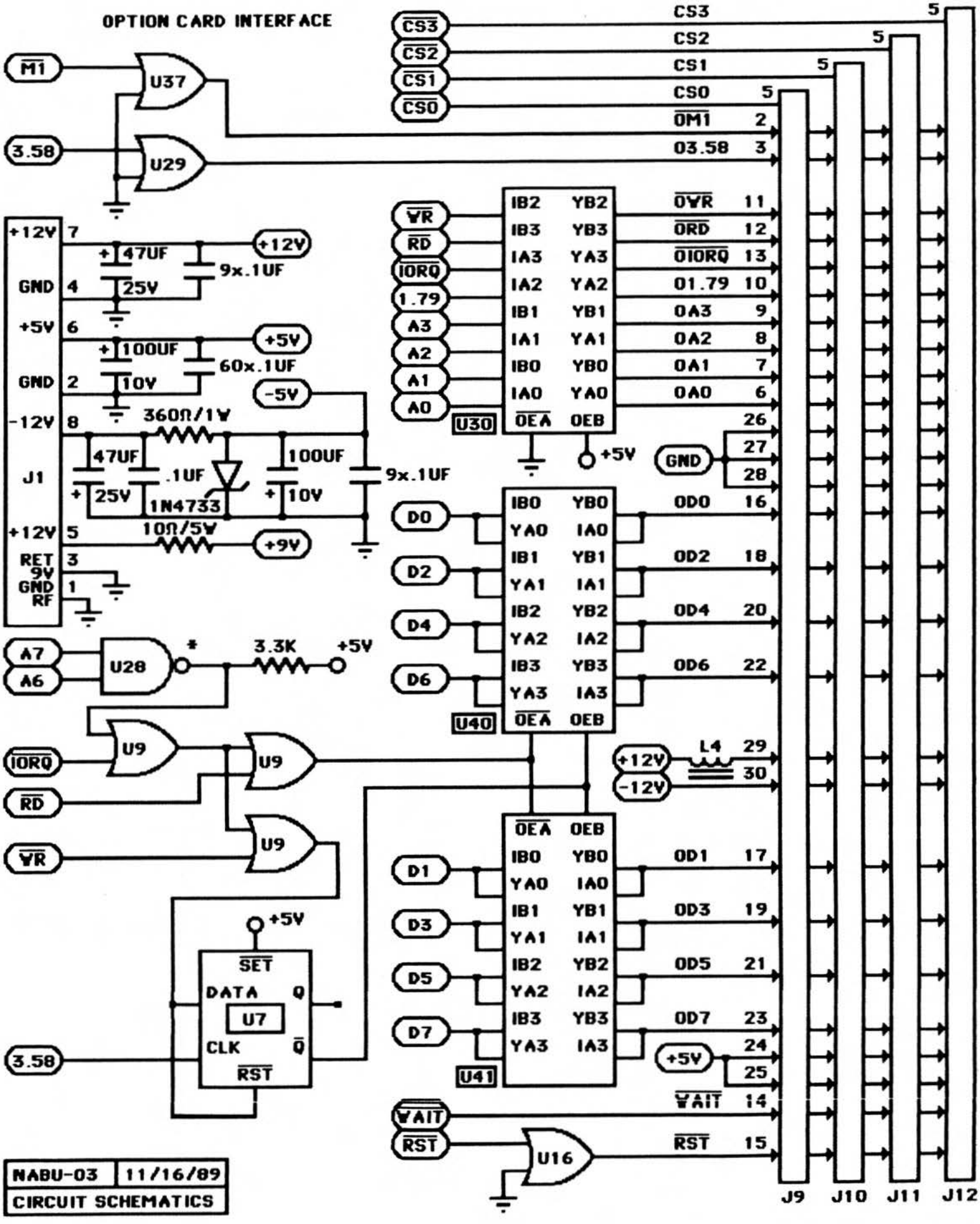


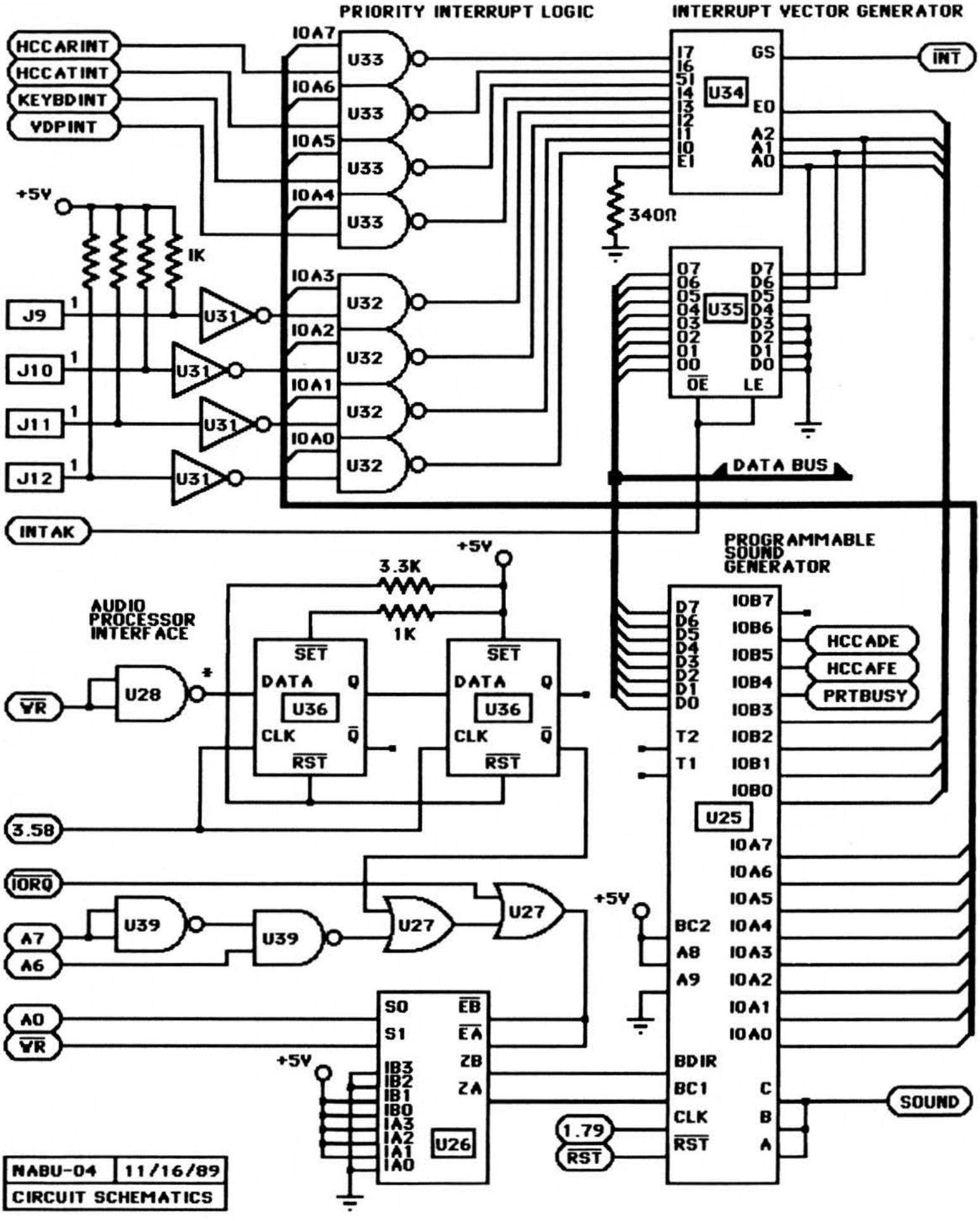
NABU MEMORY MAP

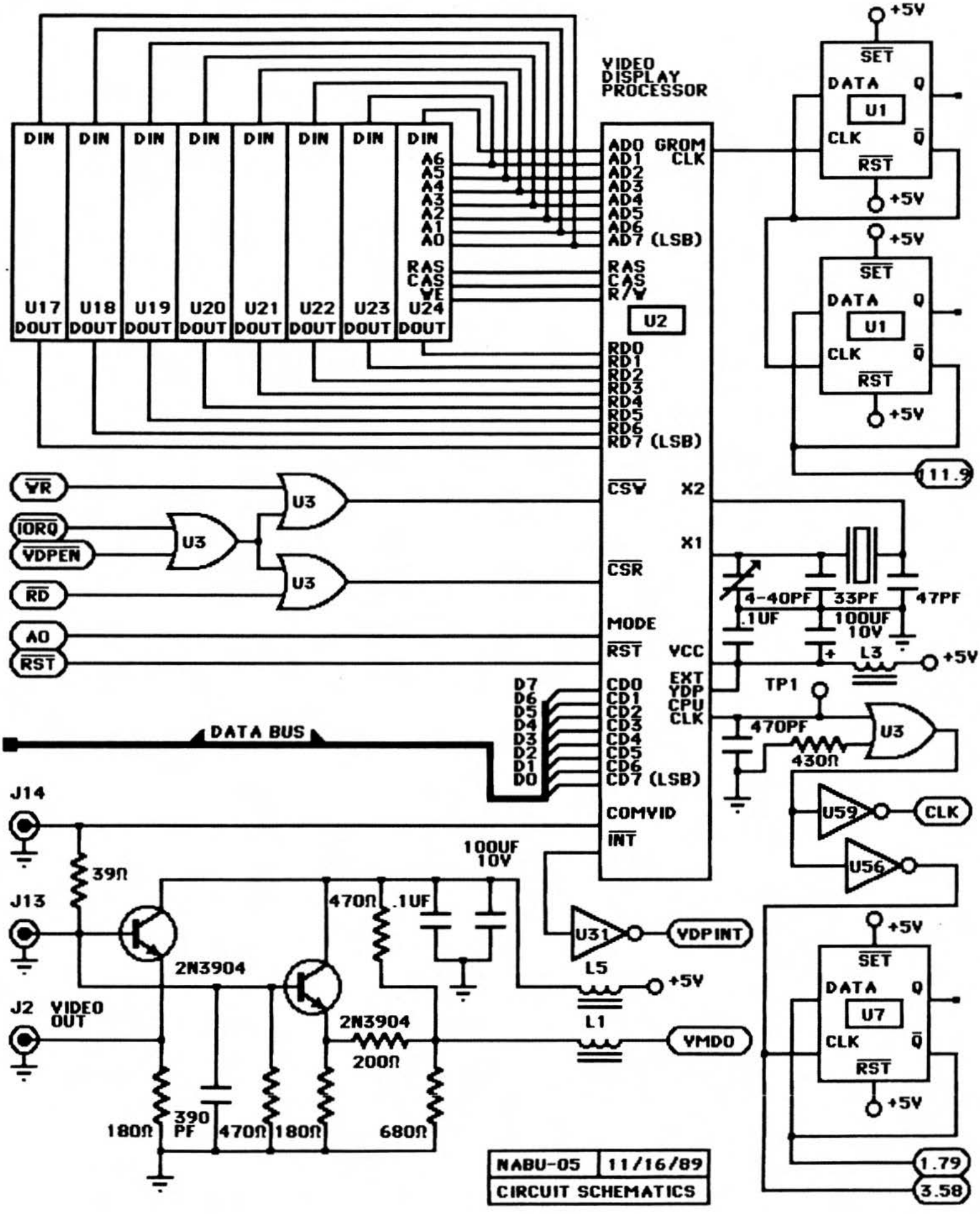
CHIP NO.	I.C. REF.	PIN NO.			
		GND	+5V	-5V	+12V
U1,U7,U36,U58	LS74	7	14		
U2	TMS9918	12	33		
U3,U8,U9,U16,U27,U29,U37,U57	LS32	7	14		
U4	8251A	4	26		
U5	7406	7	14		
U6,U11	LS273	10	20		
U10	LS138	8	16		
U12	9637	4	1		
U13	9638	4	1		
U14	TR1863P	3	1		
U15	LM3900	7			14
U17.... 24	TMS4116	16	9	1	8
U25	AY-3-8910	1	40		
U26	LS153	8	16		
U28	LS38	7	14		
U30,U40,41	LS241	10	20		
U31	LS14	7	14		
U32,U33,U39	LS00	7	14		
U34	LS348	8	16		
U35	LS373	10	20		
U38	LP76-57	7	14		
U42.... 49	HM4864-2	16	8		
U50	33Ω PACK				
U51,U52	LS157	8	16		
U53 4K EPROM	2732	12	24	...	...
U53 8K EPROM	2764	14	28		
U54	Z80A	29	11		
U55	LS260	7	14		
U56	LS04	7	14		
U59	74F04	7	14		

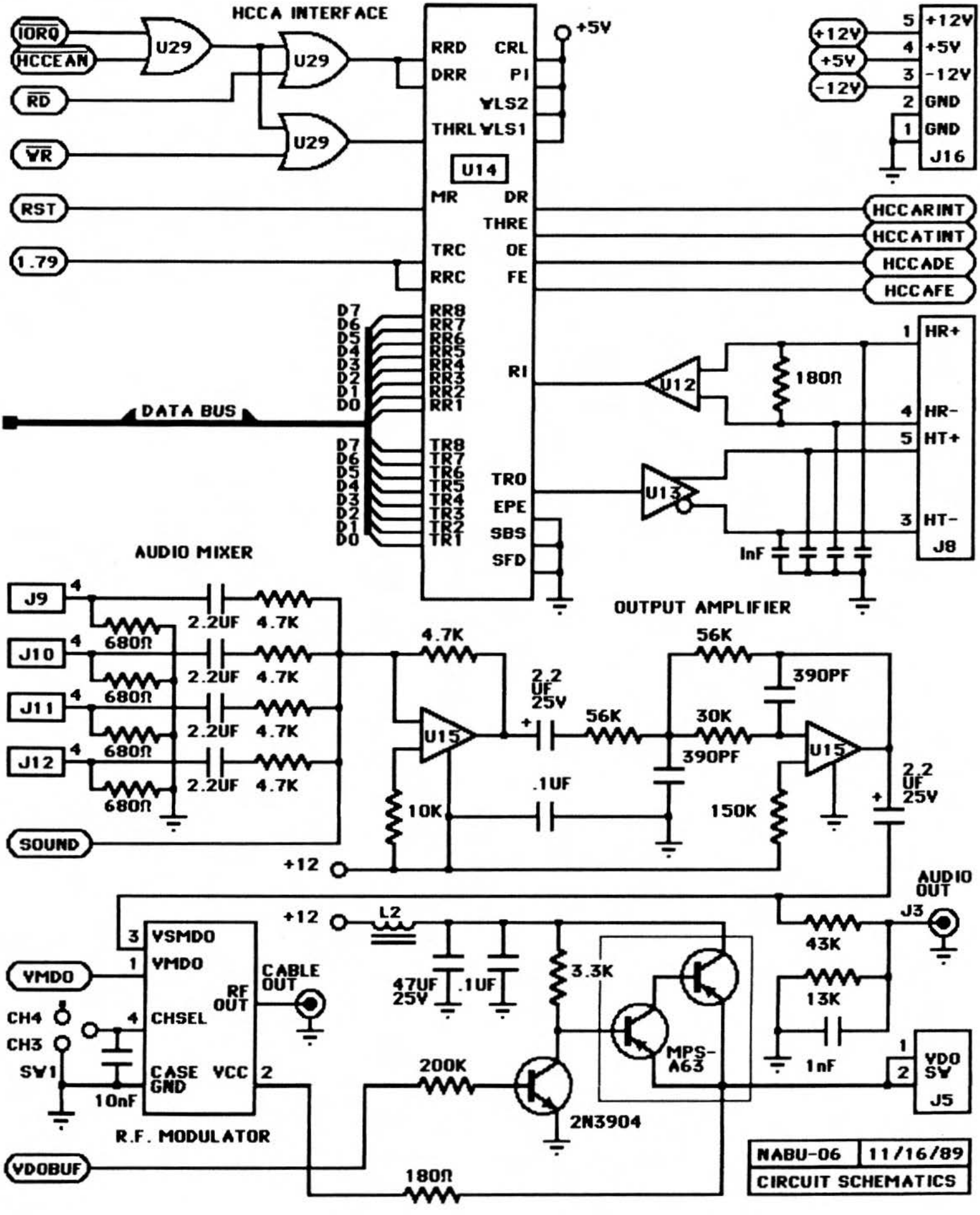

ADDR BUS
DATA BUS
4K/8K PROM
RAM ADDRESS MUX
U51
U52
U53
U54
U55
U56
U57
U58
U39
U9
U37
U38
U28
64K RAM
ROMSEL
MREQ
BUSAK
RD
BUSRQ
HALT
WR
NMI
WAIT
INT
RESET
CLK
IORQ
M1
INTAK
RFSH
VCC
GND
4K 8K
3.3K
680Ω
680PF
33Ω
20NS
60NS
WAIT STATE
DATA
SET
RST
3.58
NABU-01 | 11/16/89
CIRCUIT SCHEMATICS


ADDRESS DECODER
CONTROL REGISTER
FRONT PANEL
+5V
4 +5V
3 LED3
2 LED2
1 LED1
8 N.C.
7 N.C.
6 GND
5 RST
J15
200Ω
300Ω
200Ω
U5
U5
U5
U5
A6 A2 07 CS3
A5 A1 06 CS2
A4 A0 U10 05 CS1
A7 E3 04 CS0
03 PRTEN
02 YDPEN
E2 01 KEYBDEN
E1 00 HCCAEN
D7 D3 Q3
D6 D4 Q4
D5 D2 Q2
D4 D5 Q5
D3 D1 U6 Q1
D2 D6 Q6
D1 D0 Q0
D0 D7 Q7
MR
CLK
VDOBUF
ROMSEL
ADDR BUS
DATA BUS
RESET LOGIC
+5V
10K
240Ω
1N914
47UF 25V
U31
U56
1 RST SW
2
J6
RST
RST
A7
A6
U27
U8
U8
PRTBUSY
A0
PRTEN
U27
U8
+5V
3.3K
10 +5V
1 STB
11 BUSY
1nF 9 D7
1nF 8 D6
1nF 7 D5
1nF 6 D4
1nF 5 D3
1nF 4 D2
1nF 3 D1
1nF 2 D0
15 GND
J7
KEYBDEN
IORQ
U8
C/D
CS
U4
RST
RD
WR
RxC
CLK
CTS
DSR
RxD
RxRDY
D7 D6 D5 D4 D3 D2 D1 D0
DTR RTS TxC TxEMT TxD TxRDY
RST
RD
WR
111.9
1.79
CLK
D7 D4 Q4
D6 D3 Q3
D5 D5 Q5
D4 D2 Q2
D3 D6 U11 Q6
D2 D1 Q1
D1 D7 Q7
D0 D0 Q0
MR
+5V
PARALLEL PRINTER INTERFACE
+KR 4
-KR 5
+8V 3
GND 2
J4
180Ω
U12
+8V
1nF 1nF 1nF
SERIAL KEYBOARD INTERFACE
KEYBDINT
NABU-02 11/16/89
CIRCUIT SCHEMATICS


OPTION CARD INTERFACE
M1
U37
3.58
U29
CS3
CS2
CS1
CS0
OM1
03.58
+12V 7
GND 4
+5V 6
GND 2
-12V 8
J1
+12V 5
RET 9V 3
GND RF 1
47UF
25V
9x.1UF
100UF
10V
60x.1UF
360Ω/1W
.1UF
1N4733
10Ω/5W
+9V
-5V
WR
RD
IORQ
1.79
A3
A2
A1
A0
U30
OWR
ORD
OIORQ
01.79
OA3
OA2
OA1
OA0
OEA
OEB
+5V
GND
D0
D2
D4
D6
U40
OD0
OD2
OD4
OD6
A7
A6
U28
3.3K
U9
L4
D1
D3
D5
D7
U41
OD1
OD3
OD5
OD7
SET
DATA
U7
CLK
RST
WAIT
U16
J9
J10
J11
J12
NABU-03 | 11/16/89
CIRCUIT SCHEMATICS


PRIORITY INTERRUPT LOGIC
INTERRUPT VECTOR GENERATOR
HCCARINT
HCCATINT
KEYBDINT
VDPINT
IOA7
IOA6
IOA5
IOA4
IOA3
IOA2
IOA1
IOA0
U33
U32
U34
U35
U31
+5V
1K
340Ω
J9
J10
J11
J12
INT
INTAK
DATA BUS
AUDIO PROCESSOR INTERFACE
3.3K
1K
SET
DATA
CLK
RST
U36
U28
U39
U27
3.58
IORQ
WR
PROGRAMMABLE SOUND GENERATOR
U25
HCCADE
HCCAFE
PRTBUSY
SOUND
1.79
RST
U26
NABU-04 | 11/16/89
CIRCUIT SCHEMATICS


VIDEO DISPLAY PROCESSOR
DIN
A6
A5
A4
A3
A2
A1
A0
RAS
CAS
WE
U17 DOUT
U18 DOUT
U19 DOUT
U20 DOUT
U21 DOUT
U22 DOUT
U23 DOUT
U24 DOUT
U2
AD0 GROM CLK
AD1
AD2
AD3
AD4
AD5
AD6
AD7 (LSB)
RAS
CAS
R/W
RD0
RD1
RD2
RD3
RD4
RD5
RD6
RD7 (LSB)
+5V
SET
DATA
Q
U1
CLK
RST
11.9
VR
IORQ
VDPEN
RD
U3
CSW
CSR
X2
X1
4-40PF
33PF
47PF
.1UF
100UF 10V
MODE
RST
VCC
L3
A0
EXT VDP CPU CLK
TP1
D7
D6
D5
D4
D3
D2
D1
D0
CD0
CD1
CD2
CD3
CD4
CD5
CD6
CD7 (LSB)
DATA BUS
470PF
430Ω
U59
CLK
U56
J14
COMVID
INT
39Ω
J13
100UF 10V
470Ω
.1UF
2N3904
U31
VDPINT
L5
J2 VIDEO OUT
L1
VMDO
200Ω
180Ω
390 PF
680Ω
U7
1.79
3.58
NABU-05
11/16/89
CIRCUIT SCHEMATICS


HCCA INTERFACE
IORQ
HCCEAN
RD
WR
RST
1.79
U29
U29
U29
U14
RRD
DRR
CRL
PI
WLS2
WLS1
THRL
MR
DR
THRE
TRC
OE
RRC
FE
RR8
RR7
RR6
RR5
RR4
RR3
RR2
RR1
RI
TR8
TR7
TR6
TR5
TR4
TR3
TR2
TR1
TRO
EPE
SBS
SFD
+5V
DATA BUS
D7
D6
D5
D4
D3
D2
D1
D0
+12V
+5V
-12V
5 +12V
4 +5V
3 -12V
2 GND
1 GND
J16
HCCARINT
HCCATINT
HCCADE
HCCAFE
U12
U13
180Ω
1 HR+
4 HR-
5 HT+
3 HT-
J8
1nF
AUDIO MIXER
J9
J10
J11
J12
SOUND
4
680Ω
2.2UF
4.7K
OUTPUT AMPLIFIER
U15
4.7K
2.2 UF 25V
56K
390PF
30K
390PF
.1UF
10K
150K
+12
AUDIO OUT
J3
43K
13K
1nF
3.3K
MPS-A63
2N3904
200K
180Ω
L2
47UF 25V
.1UF
VSMDO
VMDO
CHSEL
RF OUT
CABLE OUT
CASE
GND
VCC
CH4
CH3
SW1
10nF
R.F. MODULATOR
VDOBUF
VDO SW
J5
NABU-06
11/16/89
CIRCUIT SCHEMATICS